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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Paper No. 16

Application Number: 09/517,518
Filing Date: March 02, 2000
Appellants: WONG ET AL.

MAILED

DEC 0 2 2002

GROUP 2800

<u>B.Y. Mathis</u>
<u>For Appellants</u>

EXAMINER'S ANSWER

Response to Appellants' Appeal Brief filed 11 November 2002.

(1)   Real Party in Interest

A statement identifying the real party in interest as Advanced Micro Devices, Inc.

is contained in the brief.

(2)   Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly

affect or be directly affected by or have a bearing on the decision in the pending appeal

is contained in the brief.

(3)   Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4)   Status of Amendments After Final

The Appellants' statement of the status of amendments after final rejection

contained in the brief is correct. All amendments have been entered.

(5)   Summary of Invention

The summary of invention contained in the brief is correct.

(6)   Issues

The Appellants' statement of the issues in the brief is correct.

(7)   Grouping of Claims

The Appellants' statement in the brief that certain claims do not stand or fall

together is contested because some of the claims listed by Appellants are dependent

claims and are not separately patentable. Additionally, Appellants did not provide

argument based on the claim grouping asserted.

(8)   Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9)   Prior Art of Record

6,295,636   DUPENLOUP   09-2001

(10)   Grounds of Rejection

The following ground of rejection remains applicable to the appealed claims:

Claims 1-3 and 5-17 stand rejected under 35 U.S.C. 102(e) as anticipated by

Dupenloup, U.S. Patent 6,295,636. The Final office action, Paper No. 11, sets forth this

rejection in toto.   Independent and representative claim 1 is reproduced below together

with the corresponding citations from Dupenloup used to reject its claim limitations.

Claim 1	
A method of synthesizing a register transfer level (RTL) based design of a system . . .	column 4, lines 28-32; column 3, lines 20-23.
determining a plurality of sub-modules of a top level system;	column 4, lines 4-12.
determining individual time budgets for each sub-module based on timing requirements of the top-level system;	Figure 19; see also column 43, lines 8-15.
synthesizing gate-level designs of the sub-modules based on the determined time budgets for the individual sub-modules;	Figure 19; column 43, lines 16-21.
testing the gate-level designs for conformance with gate-level design requirements of the individual sub-modules, then integrating the gate-level designs of the individual sub-modules to form a top level design;	Figure 19, #s 451, 452, 455. column 41, lines 1-13.
testing the top-level design for conformance with top-level design requirements; and	Figure 19; #s 451, 452, 455.
generating a top-level netlist when the top-level design conforms to the top-level design requirements.	Figure 19, #456.

(11) *Response to Argument*

I. Introduction

The prior art, Dupenloup, anticipates Appellants' claims and meets the requirements for rejecting claims 1-3 and 5-17 under 35 U.S.C. § 102. Appellants correctly state that a 35 U.S.C. 102 rejection requires the identical disclosure in a single reference of each element of a claimed invention. However, "identical disclosure" does not require a verbatim or word-for-word equivalence, i.e. the test of anticipation is not an "ipsissimis verbis" test. **In re Bond**, 15 U.S.P.Q. 2d, 1566 (Fed. Cir. 1990). Consideration being given to this principle, Dupenloup includes and teaches all the elements of Appellants' claimed limitations.

Appellants' arguments revolve around Appellants' primary contention that the Dupenloup prior art does not apply to design sub-modules. However, the facts of Dupenloup disclose otherwise.

II. **Dupenloup Teaches Testing Of Individual Sub-Modules**

Dupenloup discloses a method of synthesizing integrated circuit (IC) designs and generating logic synthesis scripts for modules and sub-modules of an IC design. As succinctly stated in the Abstract of Dupenloup, the method discloses

> [g]enerating script to cause a logic synthesis tool to apply bottom-up synthesis to **modules and sub-modules** of the IC design, generating script to cause a logic synthesis tool to apply top-down characterization to modules and sub-modules of the IC design and generating script to cause a logic synthesis tool to repeat said bottom-up and said top-down applications until certain predetermined constraints are satisfied. (emphasis added).

Dupenloup's method, therefore, applies to IC circuit modules and sub-modules.

Dupenloup's Figure 1, reproduced below, illustrates the overall IC design cycle.

FIG. 1

<u>DESIGN CYCLE</u>
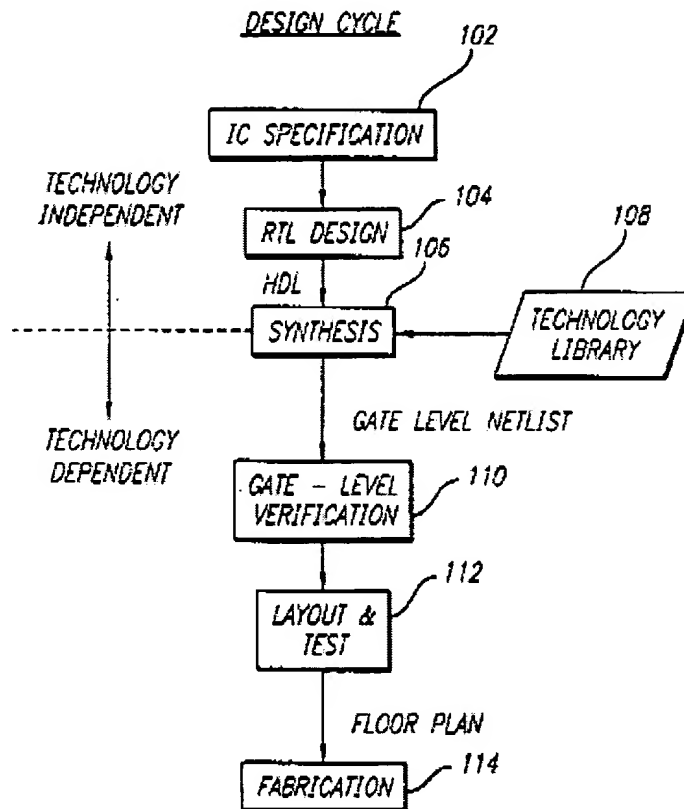
At step 104, supra, the RTL design exists. With reference to this step,

Dupenloup states at column 2, lines 19-22:

> At the RTL level, designers must take (sic) all key design decisions such
> as design hierarchy and partitioning, clocking scheme, reset scheme, and
> locations of registers. All those decisions are contained and reflected in
> the RTL code.

In sum, at the RTL Design level, partitioning of the design occurs resulting in a

design hierarchy of design modules *and* submodules. The establishment of

design modules and submodules subsequent to a partitioning process is a

fundamental principle inherent to the art of IC design.

Referring again to Figure 1, supra, at step 106, synthesis of the design

modules/submodules occurs and the result is a gate level netlist. Next, step 110

depicts "Gate-Level Verification". Verification and test are synonymous terms in

the art of IC design.

Appellants cite to Dupenloup at column 43, lines 10-16 which details

testing for a gate level design. Now dissecting this cite, the first sentence reads:

> Referring to Figure 19, the interactive improvement process begins with
> initial mapping utilizing bottom-up synthesis techniques with each module
> being assigned default constraints, time budgets, and clock definitions.

Dupenloup's Figure 19, step 454, illustrates the synthesis process.

FIG. 19
SYNTHESIS
PROCESS
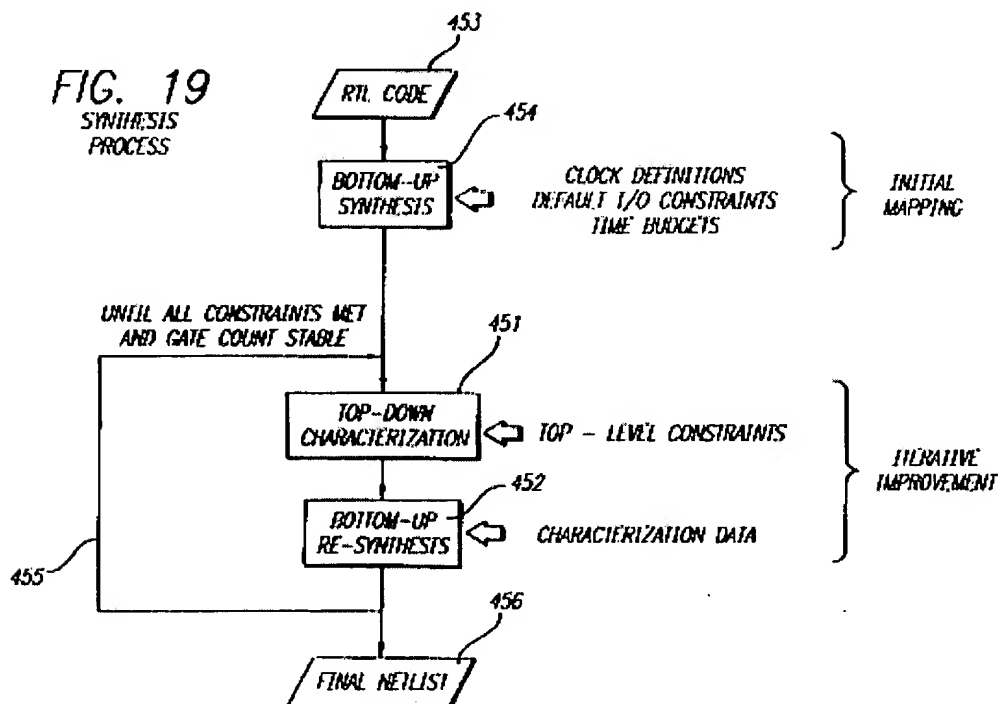
The result of the synthesis process, albeit not as explicitly shown in Figure 19 as it was shown in Figure 1, is a gate level netlist. In the art of IC design, generation of a gate-level netlist is an inherent by-product of synthesis.

The Dupenloup passage at column 43 further discusses the characterization of *each* module. Column 43, lines 16-18 states:

> Top-down characterization provides constraints, time budgets, and other information required to be met by *each* of the modules. (emphasis added).

Here, Dupenloup's use of the word "each" signifies that Dupenloup applies to IC design sub-modules and modules. "[E]ach of the modules" broadly references modules and/or submodules.

Dupenloup discloses the existence of a testing or verification process wherein top-down characterization and bottom-up resynthesis are conducted until all constraints are met and the gate count is stable. Column 43, lines 21-25 states:

> The top-down characterization step and bottom-up resynthesis steps are iterated until all constraints are met by each of the modules being synthesized and gate count for each of the modules are stable.

Here, Dupenloup provides evidence of the existence of a gate level implementation coupled with subsequent testing through iteration of the top-down characterization and bottom-up resynthesis.

Appellants assert that "nowhere in Dupenloup does the term 'test' occur in conjunction with individual sub-modules." (Appellants' Argument, page 6). While this may be true of Dupenloup, the same also applies to Appellants' specification. Nowhere in Appellants' specification do Appellants use the term 'test' in conjunction with individual sub-modules. Appellants, like Dupenloup, reference a iterative process,

inherent to any testing procedure, of optimization and re-synthesis until specified requirements are satisfied. Appellants' own Figure 3, reproduced below, illustrates the procedure.

Figure 3

RTL synthesis and Timing Optimization Complete
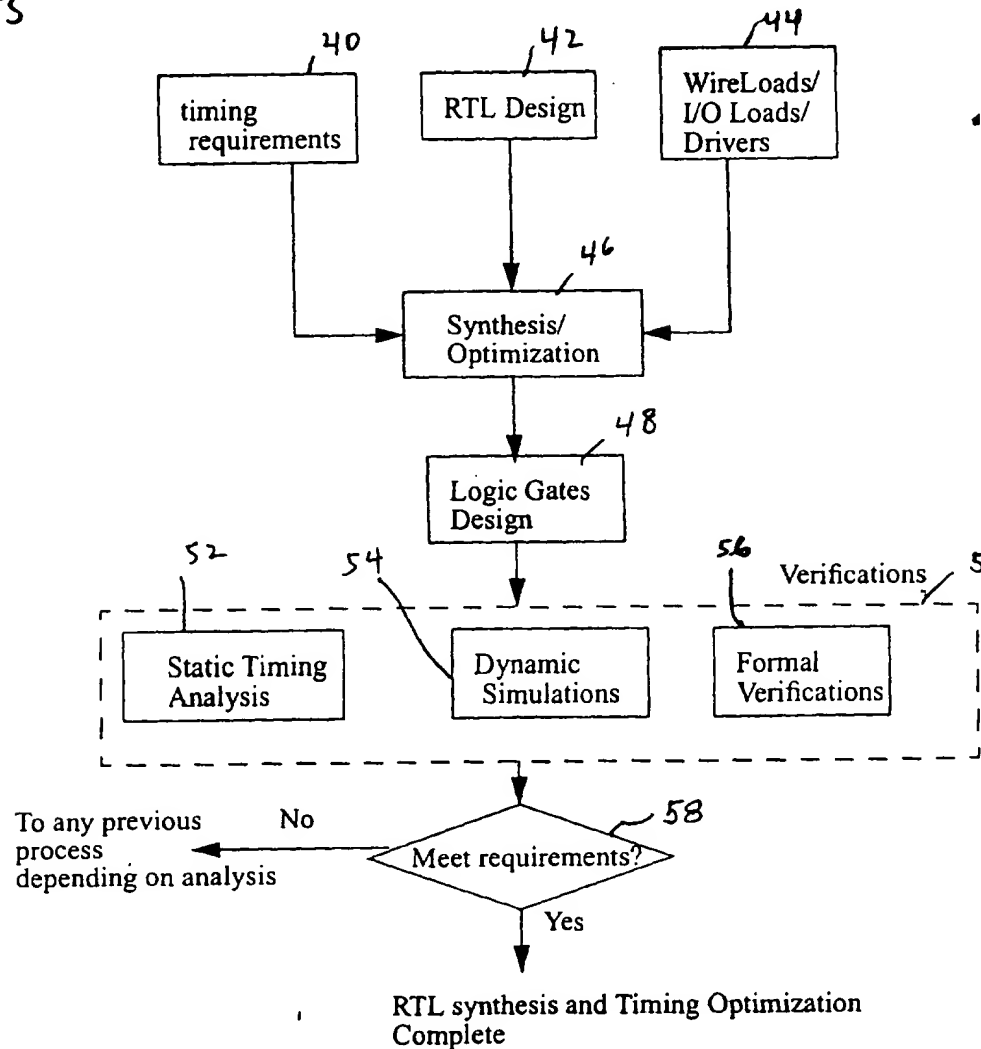
In Figure 3, steps 50 and 58 illustrate an iterative process which is considered an iterative testing procedure in the art of IC design. These steps, shown in Appellants' Figure 3, are tantamount to the Dupenloup iterative process at steps 451, 452, and 455 in Dupenloup's Figure 19, supra. Furthermore, although Appellants claim limitation

recites "testing the gate-level designs for conformance. . .", Appellants specification does not limit "testing" to any specific simulation or procedure. In fact, as previously stated, Appellants' specification does not reference or use the word "test". Rather, Appellants, as in Dupenloup, use the word "verification" and disclose a testing procedure.

Appellants further assert in argument (page 6) that determining individual time budgets for each sub-module is unsupported by Dupenloup. However Dupenloup at column 43, lines 16-18 states in relevant part: "Top-down characterization provides constraints, **time budgets**, and other information to be met by **each** of the modules." "Modules", broadly construed in Dupenloup, also means sub-modules. Therefore, based on this Dupenloup cite, time budgeting applies to modules and sub-modules.

III. Dupenloup Teaches Generating Gate-Level Netlists for Sub-Modules

Appellants additionally argue that Dupenloup does not teach or suggest a method of synthesizing an RTL-based design of a system including generating gate-level netlists for the gate-level designs of each of the sub-modules, and integrating the gate-level designs of the individual sub-modules.

Dupenloup's Figure 1 and figure 19 illustrates a synthesis step. The synthesis process produces a gate-level netlist. As stated in Dupenloup's Background of the Invention at column 1, lines 34-35:

> The IC design, as expressed by the RTL code, is then synthesized to generate a gate-level description, or a netlist.

Dupenloup at column 1, lines 45-49, further states:

> [D]uring the synthesis process, the synthesis tool uses a given technology library, 108 of Figure 1, to map the technology independent RTL code into technology dependent **gate-level netlists**." (emphasis added).

Based on the foregoing cites, Dupenloup does teach the generation of gate level netlists. Furthermore, contrary to Appellants' assertion, module synthesis and netlist generation for a module are not "two separate and distinctly different activities." It is the synthesis process that generates a gate-level netlist. In Dupenloup, the synthesis process that produces the gate-level netlists is conducted for modules *and* sub-modules of the design. As previously stated, supra, Dupenloup states at column 43, lines 21-25:

> The top-down characterization step and bottom-up resynthesis steps are iterated until all constraints are met by each of the modules being synthesized and gate count for each of the modules are stable.

Here, as previously stated, supra, "modules" is used to broadly reference modules and submodules. Further support for this point is found at column 41, lines 55-59 which states:

> Top-down characterization consists in calculating all I/O conditions and constraints of **each of the modules and the sub-modules** in a hierarchical design. (emphasis added).

Additionally, Dupenloup's Figure 25, reproduced below provides an illustration of the modules and sub-modules of a design wherein "A" represents the top-level module of the design and "B" through "I" represents the submodules (leaves).

FIG. 25
MODULE PROCESSING
ORDER FOR PARALLEL
BOTTOM-UP SYNTHESIS
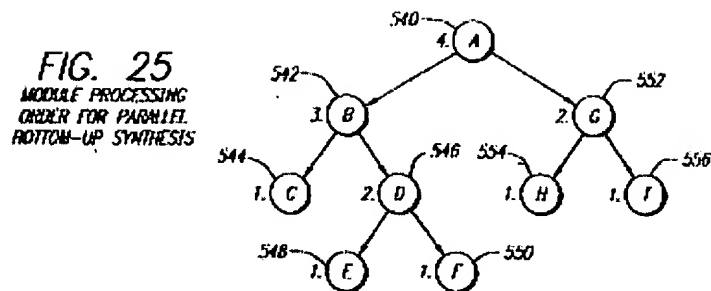
Dupenloup provides for integration of the gate level design of individual sub-

modules. Column 41, lines 6-13 provides in pertinent part:

> Synthesis then proceeds with modules that are located one level up in the
> design hierarchy. . .and the process continues until the root module . . .of
> the design is reached. Because of "don't touch" attributes, **lower level
> modules are considered as non-modifiable cells and are only
> integrated into upper levels**. This dramatically reduces the complexity
> of synthesis. (emphasis added).

Based on the foregoing citations from Dupenloup, there is nothing "erroneous"

about the rejection of claims 2, 3, 10, 11 under 35 U.S.C. 102 (e) as Dupenloup

teaches generating gate-level netlists for submodules and the integration of the

gate-level designs of the submodules.

IV. Dupenloup Teaches the Static Timing Analysis of Sub-Modules

Appellants next argue that Dupenloup does not teach or suggest a method

of synthesizing an RTL-based design of a system wherein testing gate-level

design includes performing static timing analysis on individual sub-modules for

conformance with timing requirements for individual sub-blocks. However,

Dupenloup does teach static timing analysis. One instance of this teaching may

be referenced at column 12, lines 43-48 :

From the design success prospective (sic), clock domain interfaces must be checked carefully to make sure that no timing hazard can affect the design functionality after layout and fabrication. RTL analysis extracts clock domains and clock domain interface logic. Then, the use has to analyze this data based on clock relationships.

It is the analysis of data referenced in the passage above that constitutes

the static timing analysis. Although Appellants ostensibly concede the existence

of static timing analysis in Dupenloup (Appellants state on page 8 of argument

that the [Dupenloup] passages do refer to static timing analysis), Appellants

traverse the applicability of the static timing analysis to individual sub-modules.

However, Dupenloup applies to modules and sub-modules, as explained supra,

and the Dupenloup Figures 3A, 3B, and 3C, reproduced below, are just a few of
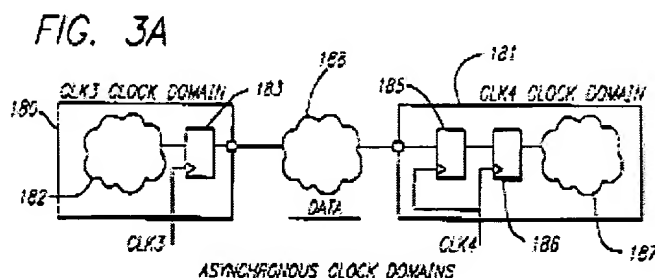
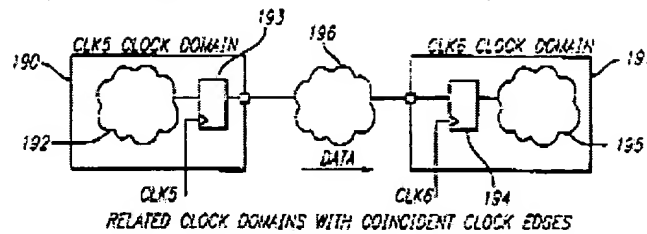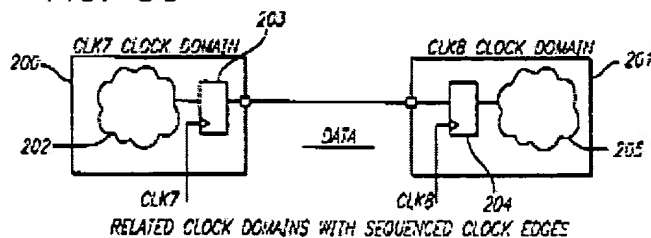the many illustrations in Dupenloup of design sub-modules.

FIG. 3A

FIG. 3B

RELATED CLOCK DOMAINS WITH COINCIDENT CLOCK EDGES

FIG. 3C

RELATED CLOCK DOMAINS WITH SEQUENCED CLOCK EDGES

V. Dupenloup Teaches the Generation of Gate-Level Netlists After Timing Requirements Of Individual Sub-Modules are met

Appellants next argue that Dupenloup does not teach or suggest a method of synthesizing an RTL-based design of a system wherein the gate-level netlists are generated for the sub-modules only if the timing requirements for the individual sub-modules are met. However, as it is well known that a picture is worth a thousand words, Dupenloup's Figure 19, reproduced supra, perfectly illustrates this limitation at steps 451, 452, and 455; in figure 19, the generation of the netlist only occurs after all constraints are met wherein the timing requirements (budget) are included in the constraints.

VI. Dupenloup Teaches Dynamic Simulations on Sub-Modules

Appellants additionally argue that Dupenloup does not teach or suggest a method of synthesizing an RTL-based design of a system having a step of
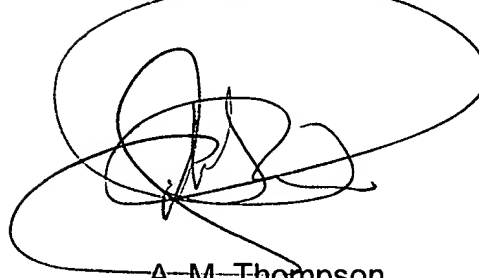
verifying conformance of the gate-level designs that includes performing dynamic simulations on the gate-level designs of individual sub-modules. However, the process of characterization disclosed in Dupenloup at column 41, lines 16-52 involves dynamic simulations. Further, Appellants' specification at page 4, lines 24-26, identifies dynamic simulations as a verification that is *typically* conducted in an RTL-based design such as Dupenloup. Therefore, even if Dupenloup did not disclose this limitation, Appellants have already conceded, and therefore it can be considered admitted prior art, that dynamic simulations are an inherent part of verification processes. Nevertheless, the rejection of Appellants' claimed limitation of performing dynamic simulations on gate-level designs of individual sub-modules is solely based on the Dupenloup disclosure and not on any admitted prior art disclosure of Appellants.

Conclusion

Having considered all of Appellants' arguments, Examiner maintains that the Dupenloup reference, at least, teaches the argued limitations of Appellants' invention. Accordingly, based on the foregoing, Examiner respectfully requests that the rejection of claims 1-3 and 5-17 under 35 U.S.C. § 102(e) as anticipated by Dupenloup be **affirmed**.

Respectfully submitted,

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November 26, 2002

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